German University in Cairo
Media Engineering and Technology

CSEN402 Computer Organization, Spring term 2020
Practice Assignment 7

Exercise 7-1

An output program resides in memory starting from address (2300)10. It is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN = 1).

a) What instruction must be placed at address 1?

Solution:

0 BUN $(2300)_{10}$

b) What must be the last two instructions of the output program?

Solution:

```
 ION
1 BUN 0 (Branch indirect with address 0)
```

Exercise 7-2

The operations to be performed with a flip-flop F (not used in the basic computer) are specified by the following register transfer statements:

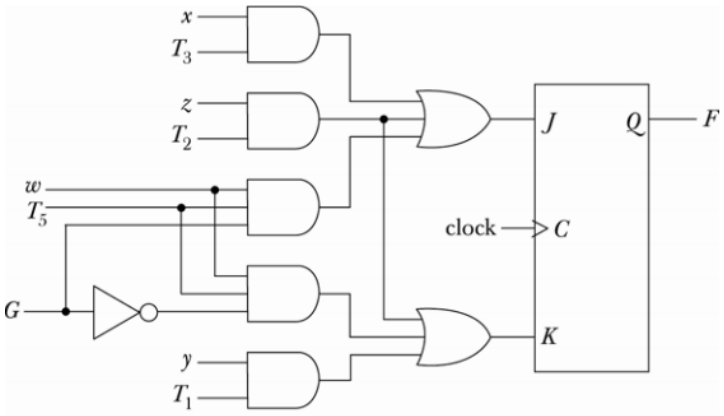
$$xT_3 : F \leftarrow 1 \text{ Set F to 1}$$
$$yT_1 : F \leftarrow 0 \text{ Clear F to 0}$$
$$zT_2 : F \leftarrow F' \text{ Complement F}$$
$$wT_5 : F \leftarrow G \text{ Transfer value of G to F}$$

Otherwise, the content of F must not change. Draw the logic diagram showing the connections of the gates that form the control functions and the inputs of flip-flop F. Use a JK flip-flop.

Solution:

$J_F = xT_3 + zT_2 + wT_5G$

$K_F = yT_1 + zT_2 + wT_5G'$



Exercise 7-3

Derive the control gates associated with the program counter PC in the basic computer.

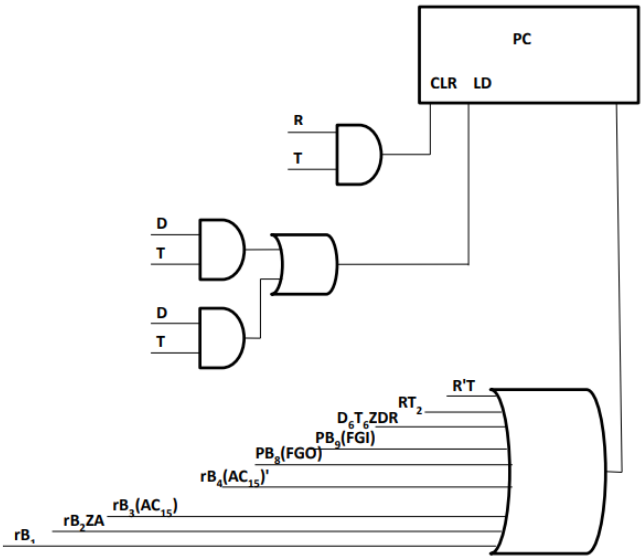
Solution:

Assume having the two variables

a) $Z_{DR} = 1$ whenever DR $= 0$

b) $Z_{AC} = 1$ whenever AC $= 0$

INR(PC) $= R'T_1 + RT_2 + D_6T_6Z_{DR} + pB_9(FGI) + pB_8(FGO) + rB_4(AC_{15})' + rB_3(AC_{15}) + rB_2Z_{AC} + rB_1E'$
LD(PC) $= D_4T_4 + D_5T_5$
CLR(PC) $= RT_1$



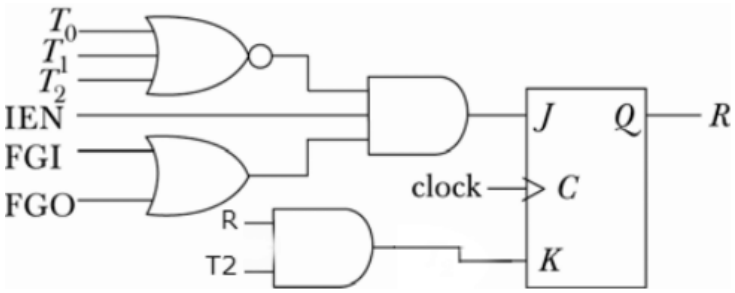
Exercise 7-4

Show the complete logic of the interrupt flip-flop R in the basic computer. Use a JK flipflop.

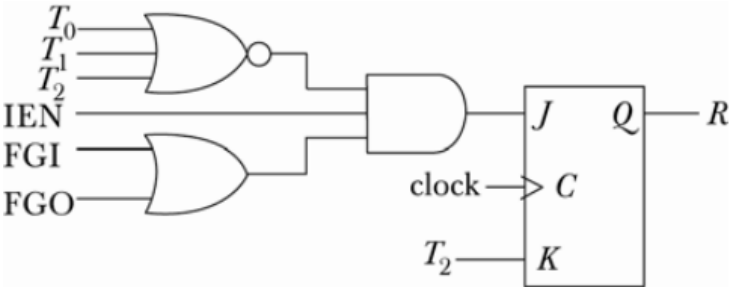
Solution:

$$(T_0 + T_1 + T_2)'(IEN)(FGI + FGO) : R \leftarrow 1$$

$$RT_2 : R \leftarrow 0$$



However it could also be done



Exercise 7-5

Derive the Boolean logic expression for x_2 (see Table 5-7). Show that x_2 can be generated with one AND gate and one OR gate.

Solution:

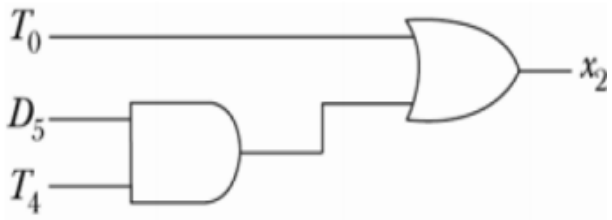
x_2 corresponds to placing PC on the bus

$$R'T_0 : AR \leftarrow PC$$

$$RT_0 : TR \leftarrow PC$$

$$D_5T_4 : M[AR] \leftarrow PC$$

$$x_2 = R'T_0 + RT_0 + D_5T_4 = (R' + R)T_0 + D_5T_4$$



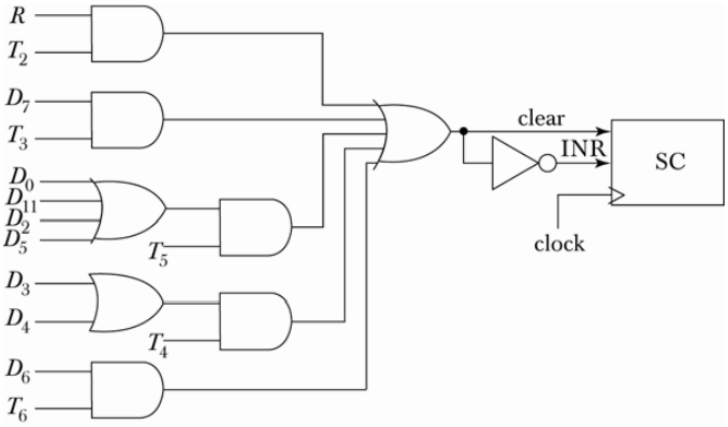
Exercise 7-6

Derive the Boolean logic expression for the gate structure that clears the sequence counter SC to 0. Draw the logic diagram of the gates and show how the output is connected to the INR and CLR inputs of SC (see Fig. 5-6). Minimize the number of gates.

Solution:

$$CLR(SC) = RT_2 + D_7T_3(I' + I) + (D_0 + D_1 + D_2 + D_5)T_5 + (D_3 + D_4)T_4 + D_6T_6$$

$$INC(SC) = otherwise$$


R
T2
D7
T3
D0
D1
D2
D5
T5
D3
D4
T4
D6
T6
clear
INR
SC
clock