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CSEN402 Computer Organization & System Programming
Spring Semester 2021
Midterm Exam

Bar Code

Instructions: Read carefully before proceeding.

1) Please tick your major

MCTR	
MET	

2) Duration of the exam: 2 hours.

3) (Non-programmable) Calculators are allowed.

4) No books or other aids are permitted for this test.

5) This exam booklet contains 13 pages, including this one and the formula sheet. Three extra sheets of scratch paper are attached and have to be kept attached. The formula sheet contains 3 pages. **Note that if one or more pages are missing, you will lose their points. Thus, you must check that your exam booklet is complete**.

6) Write your solutions in the space provided. If you need more space, write on the back of the sheet containing the problem or on the three extra sheets and make an arrow indicating that. **Scratch sheets will not be graded unless an arrow on the problem page indicates that the solution extends to the scratch sheets**.

7) When you are told that time is up, stop working on the test.

Good Luck!

Don't write anything below ;-)

Exercise	1	2	3	4	5	$\sum$
Possible Marks	20	8	20	18	12	78
Final Marks						

Exercise 1 (20 Marks)

Choose the correct answer:

a) 1- What does the micro-op $P + Q : R1 \leftarrow R2 + R3$ mean?

1. When the sum of P and Q is 1, the sum of contents of R2 and R3 is transferred to R1.
2. When the ORing of P and Q is 1, the sum of contents of R2 and R3 is transferred to R1.
3. When the sum of P and Q is 1, the ORing of contents of R2 and R3 is transferred to R1.
4. When the ORing of P and Q is 1, the ORing of contents of R2 and R3 is transferred to R1.

Solution:

When the ORing of P and Q is 1, the sum of contents of R2 and R3 is transferred to R1.

b) Which operation is identical to A-B?

1. A+B'
2. A+B-1
3. A+B'-1
4. A+B'+1

Solution:

A+B'+1

c) Consider the Operand Register $B = 11000000$ What is the result of Selective Set of register $A = 00111100$

1. 1111 1100
2. 1111 1101
3. 1111 0000
4. 0000 1111

Solution:

1111 1100

d) What is the result of the arithmetic shift right of 1001?

1. 0100
2. 1100
3. 0010
4. 0011

Solution:

1100

e) Consider a memory containing 1024 words with each word being 64 bits. How many bits should the address line be?

1. 6
2. 10
3. 16
4. 12

Solution:

10

f) A computer with 16 registers, each register being 8 bits. If the bus is implemented using multiplexers, how many multiplexer(s) are needed?

1. 8
2. 16
3. 128
4. 1

Solution:

8

g) A computer with 16 registers, each register being 8 bits. If the bus is implemented using multiplexers, What is the size of each multiplexer?

1. 8-to-1
2. 16-to-1
3. 2-to-1
4. 4-to-16

Solution:

16-to-1

h) A computer with 16 registers, each register being 8 bits. If the bus uses tri-state buffer(s), how many buffers we need?

1. 8
2. 16
3. 128
4. 1

Solution:

128

i) We wish to add the value currently present in address 2607 (decimal) in memory to the accumulator. What is the instruction needed in hex? (You can use the formula sheet)

1. 1A2F
2. 9A2F
3. 12067
4. 92067

Solution:

1A2F

j) Which statement(s) is/are correct? Choose all correct answers.

1. The AR and the IR registers should have the same size
2. The PC and the IR registers should have the same size
3. The PC and the AR registers should have the same size
4. The DR and the AC registers should have the same size

Solution:

the PC and the AR registers should have the same size
The DR and the AC registers should have the same size

Exercise 2 (8 Marks)

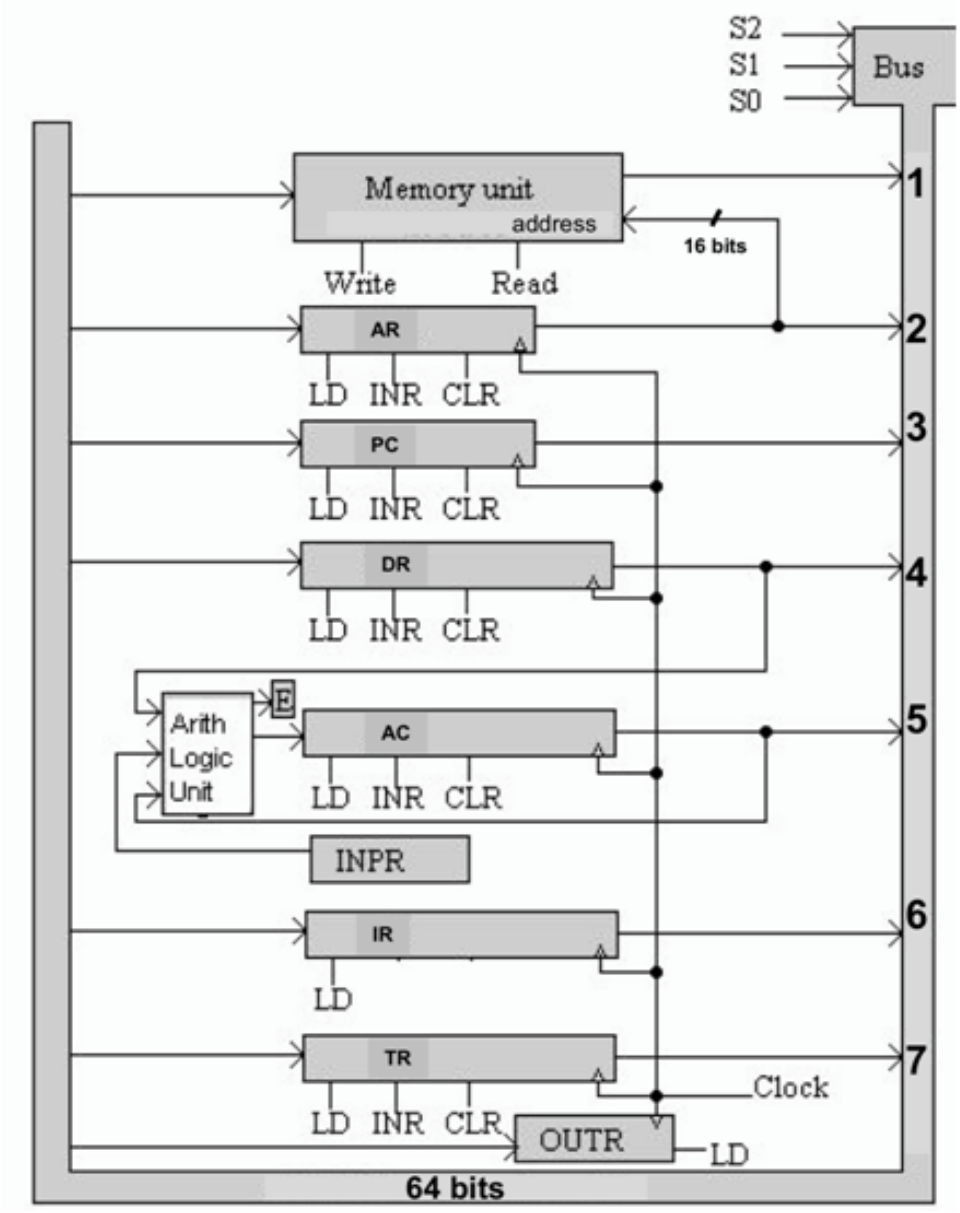
Consider a basic computer with memory reference instructions only. How many bits should the IR register be if the memory of size 768 bytes, each word is 24 bits, 32 different memory operations are available, and 2 addressing modes. Show your work and the different sections of the IR with their respective sizes.

Solution:

Memory: 768 bytes / (3 bytes per word) = 256 words thus 8 bits for address
32 different operations thus5 bits needed (opcode)
2 addressing modes thus 1 bit needed (I-bit)
Total: 14 bits.

Exercise 3 (20 Marks)

Consider this version of the modified basic computer.



Answer the below questions:

a) What is the size of the AR register?

Solution:

16 bits

b) What is the size of the memory?

Solution:

The bus is 64 bits which means memory words are 64 bits or 8 bytes, and with 16 bits address it means $2^16 words$ Thus size $2^16x8 = 524288$ bytes or 512 KB

c) What is the size of the DR register?

Solution:

64 bits

d) List any control values (memory controls, loads, increments, clear, and the bus controls S2, S1 and S0) and the ALU function to achieve each of the following in one clock cycle. If it is not possible state why

1. AR ← PC, PC ← PC +1

   Solution:
   $S_2S_1S_0 = 011$
   LD of AR = 1
   INR of PC = 1

2. TR ←M[AR], AC ←DR

   Solution:
   $S_2S_1S_0 = 001$
   Memory read=1
   LD of TR = 1
   LD of AC=1
   ALU set to transfer the DR value to AC

3. $M[AR] \leftarrow DR \wedge AC$

   Solution:
   no it's not possible because first we need to load the AC with the DR AC using load of AC and ALU set to ANDing, then in the next cycle, we need to set the write of memory to 1 and bus control to 101.

e) Sometimes we want to branch to a relative address which is calculated by adding a value (currently in DR) to the PC and place the result into the address register AR. Can we do AR $\leftarrow$ PC + DR in one clock cycle? Why or why not? Is yes, state all the needed control signals for the regisers and the bus and the ALU and memory. If not, what are the steps that should be done in the minimum clock cycles possible? List all controls needed in each clock cycle.

Solution:

We can't because PC is not connected to the ALU and hence we cannot add it to the DR and transfer it to AR in one clock cycle.

Solution to the problem is by having this in several clock cycles.

Cycle 1: transfer the DR to AC by enabling the LD of the AC, S = 100 and ALU set to transfer operation.

Cycle 2: transfer PC to DR, by setting S = 011 and LD of DR = 1.

Cycle 3: set LD of AC to 1 and set ALU to addition between DR and AC.

Cycle 4: enable the LD of AR register and S=101

f) We wish to modify this basic computer by adding an additional memory and two new registers:DR_2 and AR_2 The new memory is addressed using the AR_2 register and has its own read and write controls. Modify the above diagram of the basic computer. Draw the new diagram highlighting the changes/additions done.

Solution:

With the addition of a memory and 2 new registers, we need to increase the S control lines of the bus to 4 lines since now we have 10 components competing for the bus instead of 7.

Exercise 4 (18 Marks)

Assume that the contents of the memory of the basic computer is as shown in this table. Addresses are given in hexadecimal. Initially, AC = 0014_{16}, DR=0000_{16} and PC=001_{16}. All numbers should be shown in hexadecimal.

Consider that the below instructions form a program.

#001	0111001000000000
#002	0111000000100000
#003	0001000000001000
#004	0111000000010000
#005	0111100000000000
#006	0011001100100000
#007	0111000000000001
#008	0000000000011110

a) Show the contents of each of the registers AC, PC, AR, DR, IR, and the I flip-flop (bit) **after each instruction**. You do not need to show the changes at every clock cycle, only at the end of executing an instruction.

Instruction	AC	PC	AR	DR	IR	I

Solution:

Instruction	AC	PC	AR	DR	IR	I
Initial	0014	001	-	0000	-	-
001	FFEB	002	200	0000	7200	0
002	FFEC	003	020	0000	7020	0
003	000A	004	008	001E	1008	0
0004	000A	006	010	001E	7010	0
0006	000A	007	320	001E	3320	0
0007	000A	008	001	001E	7001	0

b) Translate the instructions into a program using any language of your choice such as Java, Python or C code, ... etc.

Solution:

```
AC = 30 - AC;
if (AC=<0)
    AC=0;
```

Exercise 5 (12 Marks)

Assume that we want to replace the new memory reference operation ISZ with a new operation CompSkip that operates as follows:

It compares the value inside the AC register with the value inside a memory location

If the AC register is equal to the value inside the memory, the next operation is skipped, otherwise execution proceeds as normal

a) Specify what will be the micro-operations that have to be executed and their control signals.

Solution:

$$T_0 : AR \leftarrow PC$$

$$T_1 : IR \leftarrow M[AR], PC \leftarrow PC + 1$$

$$T_2 : Decode$$

$$IT_3 : AR \leftarrow M[AR]$$

$$T_4 D_6 : DR \leftarrow M[AR]$$

$$T_5 D_6 : AC \leftarrow AC - DR$$

$$T_6 D_6 : if AC > 0 : PC \leftarrow PC + 1$$

b) How many clock cycles will be needed to execute the instruction

Solution:

6 cycles

Scratch paper

Scratch paper

Scratch paper